WHAT IS CLAIMED IS:

1. A testing apparatus for an integrated circuit comprising:

a pattern generator built in said integrated circuit to generate test patterns;

a plurality of shift registers configured with sequential circuit elements inside said integrated circuit; and

a pattern modifier for modifying said test patterns generated by said pattern generator according to an external input, and inputting said modified test patterns to said shift registers.

2. A testing apparatus for an integrated circuit comprising:

a plurality of shift registers, to which test patterns are inputted, configured with sequential circuit elements inside said integrated circuit;

a mask for masking an indeterminate value in outputs from said shift registers; and

an output verifier for verifying output results masked by said mask.

3. A testing apparatus for an integrated circuit comprising:

a pattern generator built in said integrated

circuit to generate test patterns;

a plurality of shift registers configured with sequential circuit elements inside said integrated circuit;

a pattern modifier for modifying said test patterns generated by said pattern generator according to an external input, and inputting said modified test patterns to said shift registers;

a mask for masking an indeterminate value in outputs from said shift registers; and

an output verifier for verifying output results masked by said mask.

4. The testing apparatus according to claim 2, wherein said output verifier includes a compressing means for compressing said masked output results.

5. The testing apparatus according to claim 3, wherein said output verifier includes a compressing means for compressing said masked output results.

6. A testing method for an integrated circuit comprising the steps of:

generating test patterns by a pattern generator built in said integrated circuit;

modifying said generated test patterns according to an external input; and

inputting said modified test patterns to a plurality of shift registers configured with sequential circuit elements inside said integrated circuit.

7. The testing apparatus according to claim 1 further comprising an automatic test pattern generating unit for generating ATPG patterns and giving said ATPG patterns as said external input to said pattern modifier;

wherein said pattern generator generates pseudo random patterns as said test patterns; and

said pattern modifier modifies said pseudo random patterns on the basis of said ATPG patterns given from said automatic test pattern generating unit.

8. The testing apparatus according to claim 3 further comprising an automatic test pattern generating unit for generating ATPG patterns and giving said ATPG patterns as said external input to said pattern modifier;

wherein said pattern generator generates pseudo random patterns as said test patterns; and

said pattern modifier modifies said pseudo random patterns on the basis of said ATPG patterns given from said automatic test pattern generating unit.

9. The testing apparatus according to claim 7, wherein said pattern modifier selects a suitable combination of one pseudo random pattern and one ATPG pattern from said pseudo random patterns generated by said pattern generator and said ATPG patterns as said external input, and modifies said selected pseudo random pattern on the basis of said selected ATPG pattern.

10. The testing apparatus according to claim 8, wherein said pattern modifier selects a suitable combination of one pseudo random pattern and one ATPG pattern from said pseudo random patterns generated by said pattern generator and said ATPG patterns as said external input, and modifies said selected pseudo random pattern on the basis of said selected ATPG pattern.

11. The testing apparatus according to claim 7, wherein said automatic test pattern generating unit refers to each of said pseudo random patterns generated by said pattern generator, selects a suitable target fault according to each of said pseudo random patterns, and generates an ATPG pattern, with which said target fault can be detected, as a reference for modifying each of said pseudo random patterns.

12. The testing apparatus according to claim 8,

wherein said automatic test pattern generating unit refers to each of said pseudo random patterns generated by said pattern generator, selects a suitable target fault according to each of said pseudo random patterns, and generates an ATPG pattern, with which said target fault can be detected, as a reference for modifying each of said pseudo random patterns.

13. The testing apparatus according to claim 7 further comprising a characteristic information determining unit for comparing said pseudo random patterns generated by said pattern generator with said ATPG patterns as said external input to determine characteristic information on said pattern generator with which said pattern generator can generate pseudo random patterns analogous to said ATPG patterns;

wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit.

14. The testing apparatus according to claim 8 further comprising a characteristic information determining unit for comparing said pseudo random patterns generated by said pattern generator with said ATPG patterns as said external input to determine characteristic information on said pattern generator

with which said pattern generator can generate pseudo random patterns analogous to said ATPG patterns;

wherein said pattern generator generates said pseudo random patterns on the basis of said characteristic information determined by said characteristic information determining unit.

15. The testing apparatus according to claim 13, wherein said characteristic information is a seed value to be set to said pattern generator.

16. The testing apparatus according to claim 14, wherein said characteristic information is a seed value to be set to said pattern generator.

17. The testing apparatus according to claim 13, wherein said pattern generator is configured as a linear feedback shift register, and said characteristic information is a feedback position in said linear feedback shift register.

18. The testing apparatus according to claim 14, wherein said pattern generator is configured as a linear feedback shift register, and said characteristic information is a feedback position in said linear feedback shift register.

19. The testing apparatus according to claim 7 further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern,an execution limitation condition for limiting the execution of said compressing process;

wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation condition setting unit is satisfied.

20. The testing apparatus according to claim 8 further comprising an execution limitation condition setting unit for setting, when said automatic test pattern generating unit executes a compressing process on said ATPG pattern,an execution limitation condition for limiting the execution of said compressing process;

wherein said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when said execution limitation condition set by said execution limitation condition setting unit is satisfied.

21. The testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an

upper limit value of the number of faults to be detected with one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value.

22. The testing apparatus according to claim 20, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper limit value of the number of faults to be detected with one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when the number of detection target faults, that are compressed in said ATPG pattern by said compressing process, reaches said upper limit value.

23. The testing apparatus according to claim 21, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses.

24. The testing apparatus according to claim 22, wherein said execution limitation condition setting unit increases said upper limit value as generation

of said ATPG pattern progresses.

25. The testing apparatus according to claim 19, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value.

26. The testing apparatus according to claim 20, wherein said execution limitation condition setting unit sets, as said execution limitation condition, an upper value of a quantity of pattern modification by said pattern modifier in the case where said pattern modifier modifies one of said pseudo random patterns on the basis of one ATPG pattern, and said automatic test pattern generating unit terminates said compressing process on said ATPG pattern when a

quantity of pattern modification, performed by said pattern modifier in the case where said pattern modifier modifies said pseudo random pattern on the basis of one ATPG pattern in which detection target faults are compressed by said compressing process, reaches said upper limit value.

27. The testing apparatus according to claim 25, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses.

28. The testing apparatus according to claim 26, wherein said execution limitation condition setting unit increases said upper limit value as generation of said ATPG pattern progresses.

29. An integrated circuit including sequential circuit elements having:

a plurality of shift registers configured with said sequential circuit elements;

a pattern generator built in said integrated circuit to generate test patterns; and

a pattern modifier built in said integrated circuit to modify said test patterns generated by said pattern generator according to an external input, and inputting said modified test patterns to said shift

registers.

30. An integrated circuit including sequential circuit elements having:

a plurality of shift registers, to which test patterns are inputted, configured with said sequential circuit elements;

a mask built in said integrated circuit to mask an indeterminate value in outputs from said shift registers; and

an output verifier built in said integrated circuit to verify output results masked by said mask.

31. An integrated circuit including sequential circuit elements having:

a plurality of shift registers configured with said sequential circuit elements;

a pattern generator built in said integrated circuit to generate test patterns;

a pattern modifier built in said integrated circuit to modify said test patterns generated by said pattern generator according to an external input, and inputting said modified test pattern to said shift registers;

a mask built in said integrated circuit to mask an indeterminate value in outputs from said shift registers; and

an output verifier built in said integrated circuit to verify output results masked by said mask.

32. The integrated circuit according to claim 29, wherein said pattern generator generates pseudo random patterns as said test patterns, and said pattern modifier modifies said pseudo random patterns on the basis of ATPG patterns generated by an automatic test pattern generator and given as said external input.

33. The integrated circuit according to claim 31, wherein said pattern generator generates pseudo random patterns as said test patterns, and said pattern modifier modifies said pseudo random patterns on the basis of ATPG patterns generated by an automatic test pattern generator and given as said external input.